

REMARKS

This is in response to the Office Action dated March 26, 2004. Claims 1-10 are pending.

Applicant notes with appreciation the Examiner's allowance of claims 4 and 10.

Fig. 1 has been amended per the Examiner's suggestion.

Claim 1 stands rejected under 35 U.S.C. Section 103(a) as being allegedly unpatentable over Lab1 in view of JP 06-112289. This Section 103(a) rejection is respectfully traversed for at least the following reasons.

First, there is absolutely no showing of record indicating that the newly cited document entitled "*Physics 3 Spring 1989 – Lab 1 – Capacitance Measurements*" (Lab1) is "prior art" to the instant invention. Lab1 appears to have been found during a recent internet search by the USPTO – clearly performed well after the instant application was filed.

Importantly, there is no evidence indicating that Lab1 was "published" prior to December 12, 2000. Instead, Lab1 appears to have come from a student's lab notebook indicative of lab experiments performed at Dartmouth College – possibly in 1989. Such a lab notebook is not "prior art" to the instant application unless it was "published" or was a "printed publication" prior to December 12, 2000. Clearly, lab notebooks typically are not "printed publications" or "published" in the United States.

The USPTO has made no showing that this lab notebook (Lab1) was published prior to December 12, 2000 (the fact that it was available on the internet in 2004 is

irrelevant). This new ground of rejection is fundamentally flawed because the USPTO has made no showing that Lab1 is "prior art" under any aspect of 35 U.S.C. Section 102.

Second, even if the newly cited Lab1 was "prior art" (which it is not), the Section 103(a) rejection using the same is incorrect. Lab1 in Fig. 3 shows that if C1 is known, then a voltmeter measuring V1 and V2 can be used to measure unknown C2 based on the voltage ratio between V1 and V2. However, Lab1 fails to disclose or suggest many of the features of claim 1, including measuring a MIS structure. Apparently recognizing this flaw in Lab1, the Office Action cites Kono.

However, Kono is insufficient for the reasons set forth in the Appeal Brief dated November 10, 2003, the disclosure of which is hereby incorporated herein by reference.

Moreover, one of ordinary skill in the art if measuring the MAIS structure of Kono would never have used a contact-type device because Kono teaches directly to the contrary. In particular, Kono teaches that one of ordinary skill in the art measuring a MAIS structure as in Kono would not use a contact-type device, thereby teaching directly away from the invention of claim 1. Yet another reason why the alleged combination fails is that Kono's V_{fbMAIS} is not a capacitance structure with known capacitance. Kono discloses a single MAIS structure (the MIS is an ideal or imagined structure calculated from measurements performed on the MAIS). Drawing 2 of Kono merely shows an equivalent circuit of the device when flat band voltage (V_{fbMAIS}) is taken into account; i.e., the device still includes a single MAIS structure. The flat band voltage (V_{fbMAIS}) of Kono is not a capacitance structure at all. Thus, the Examiner's contention that V_{fbMAIS} is

a capacitance structure with known capacitance is wrong. Since V_{fbMAIS} in Kono is not even a capacitance structure with known capacitance, the reference cannot possibly disclose or suggest a capacitance structure serially connected to a MIS as required by claim 1. The single MAIS of Kono cannot have a capacitance structure with known capacitance serially connected to a MIS as required by claim 1. Kono is entirely unrelated to the invention of claim 1. The fundamental basis of the rejection is based on an incorrect interpretation of the cited reference by the Examiner.

Additionally, the MIS structure of Kono is hypothetical and calculated from the measurements performed on the MAIS structure. In other words, Kono discloses using a Metal/Air/Insulator/Semiconductor (MAIS) structure – but not directly analyzing any MIS structure. In this respect, Kono determines measurements using a MAIS, and then uses these measurements to approximate what characteristics would be of a *hypothetical* MIS. This is because, as explained above, Kono's device is not capable of analyzing a MIS structure. Accordingly, it can be seen that, contrary to claim 1, the device of Kono is not for analyzing C-V characteristics of a MIS structure having unknown capacitance. Furthermore, since Kono is actually measuring a MAIS (not a MIS), there cannot possibly be any serial connection to a MIS or measuring synthesis capacitance of a MIS as required by claim 1. Thus, it can be seen that even if the two references were combined as alleged in the Office Action, the invention of claim 1 still would not be met.

Claims 7 and 8 also are clearly patentable. First, as explained above, Lab1 is not even prior art to the invention of these claims. Second, even if the two references were

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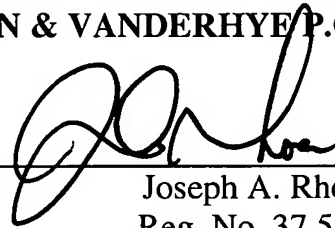
combined as alleged in the Office Action (which would be incorrect in any event), these claims still define over the cited art for the reasons discussed in the Appeal Brief dated November 10, 2003.

For at least the foregoing reasons, it is respectfully requested that all rejections be withdrawn. All claims are in condition for allowance. If any minor matter remains to be resolved, the Examiner is invited to telephone the undersigned with regard to the same.

Respectfully submitted,

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